



(19)

Europäisches Patentamt

European Patent Office

Office européen des brevets



(11)

EP 1 320 189 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
18.06.2003 Bulletin 2003/25

(51) Int Cl.7: H03B 21/00, H04B 1/40

(21) Application number: 01129616.7

(22) Date of filing: 12.12.2001

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU

MC NL PT SE TR

Designated Extension States:

AL LT LV MK RO SI

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(54) Multi-band frequency synthesiser for mobile terminals

(57) A frequency synthesiser arrangement for generating signals with frequencies for UMTS and GSM/GPRS frequency bands and a mobile terminal with a respective frequency synthesiser arrangement are proposed, comprising a reference frequency source for providing a signal of constant reference frequency, a first frequency synthesiser sub-unit for transforming the signal of the reference frequency source into a signal with a frequency in a range of a first type of frequency band, a second frequency synthesiser sub-unit for transform-

ing the signal of the reference frequency source into a signal with a frequency in a range of a second type of frequency band, whereby the second frequency synthesiser sub-unit further transforms the signal of the reference frequency source into a signal with an intermediate frequency, and a third frequency synthesiser sub-unit transforms the signal of the reference frequency source into an auxiliary signal with a fixed frequency which is used together with the signal of intermediate frequency for generating signals with frequencies in a range of a third and of a fourth type of frequency band.

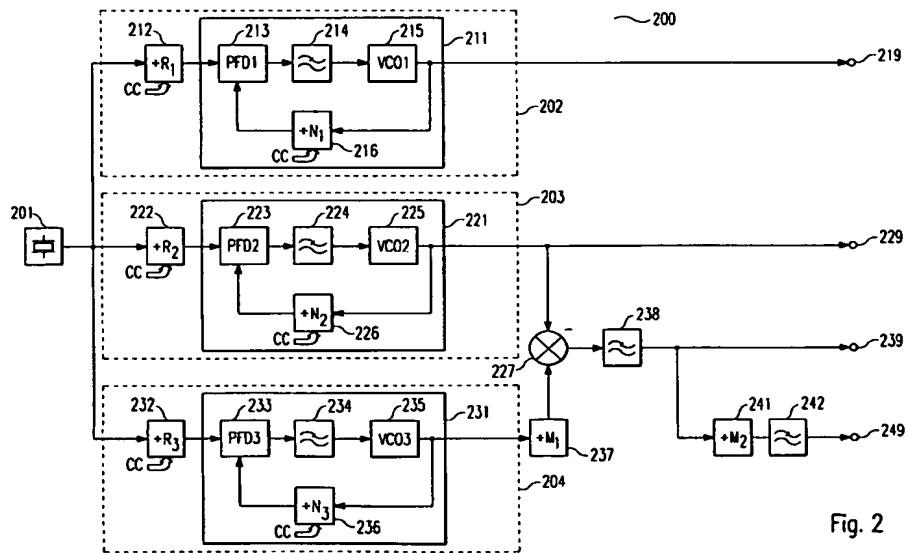


Fig. 2

Description

[0001] The present invention refers to frequency synthesisers, in particular to multi-band frequency synthesisers used in mobile terminals for wireless telecommunication networks.

5 [0002] New generation mobile terminal are equipped to support data transmission on UMTS (Universal Mobile Telecommunications System) and GSM/GPRS (Global System for Mobile Communication/General Packet Radio Services) frequency bands in one body. Therefore multi-band frequency synthesiser are required which support UMTS-FDD (UMTS-Frequency Division Duplex) and UMTS-TDD (UMTS-Time Division Duplex) frequency bands as well as triple bands functionality (GSM900/DCS1800/PCS1900 MHz) for GSM/GPRS in both up- (T_x) and down-link (R_x) directions.

10 DCS hereby stands for Digital Cellular System and PCS for Personal Communications Service.

[0003] Today's known implementations of multi-band frequency synthesisers are based on the usage of independent frequency synthesisers, one for UMTS - up-link, one for UMTS-down-link and a third one for triple band GSM/GPRS. To achieve the necessary class 12 settling time for GPRS (below 150 μ s) Fractional-N synthesisers are commonly used.

15 [0004] The biggest advantage of Fractional-N frequency synthesisers is their fast settling time when e.g. switching from an up-link to a down-link frequency band or at an intersystem handover, which fulfils one of the preconditions for a reliable GPRS data transmission. The biggest disadvantage of all classes of Fractional-N frequency synthesisers is their bad output spectrum performance which is characterised by high phase noise and a high amount of spurious spectra. Especially when receiving low-level signals, this can be very problematic. When using Fractional-N frequency synthesisers, the requirements of GSM standard 0505 can only be achieved by post-processing the output spectra 20 with high-quality filters, which are bulky and cost-intensive. This collides with the general requirements for a compact design of mobile terminals not leaving much space for bulky components, and for cost-effective technical solutions.

[0005] It is therefore an object of the present invention to propose a cost-effective multi-band frequency synthesiser with minimal space requirements but with a short settling time and with very low phase noise and a very low portion of spurious spectra.

25 [0006] This object is achieved by a frequency synthesiser arrangement and a mobile terminal as claimed in the respective independent claims.

[0007] In particular, the above object is achieved by a frequency synthesiser arrangement for generating signals with frequencies for UMTS and GSM/GPRS frequency bands, comprising a reference frequency source for providing a signal of constant reference frequency, a first frequency synthesiser sub-unit for transforming the signal of the reference frequency source into a signal with a frequency in a range of a first type of frequency band, a second frequency synthesiser sub-unit for transforming the signal of the reference frequency source into a signal with a frequency in a range of a second type of frequency band, whereby the second frequency synthesiser sub-unit further transforms the signal of the reference frequency source into a signal with an intermediate frequency, and a third frequency synthesiser sub-unit transforms the signal of the reference frequency source into an auxiliary signal with a fixed frequency, i.e. small frequency range, which is used together with the signal of intermediate frequency for generating signals with frequencies in a range of a third and of a fourth type of frequency band.

30 [0008] The first, second, third and fourth type of frequency bands are different from each other and correspond to the frequency bands necessary for different wireless communication standards. In particular, the first type of frequency band supports the UMTS TDD1, FDD- T_x and TDD2 standards, the second type of frequency band supports the UMTS FDD- R_x standard, the third type of frequency band supports the GSM/GPRS 1800/1900MHz standards DCS and PCS, and the fourth type of frequency band supports the GSM 900MHz standard.

35 [0009] The above object is further achieved by a mobile terminal for use with UMTS and GSM/GPRS frequency bands with a frequency synthesiser arrangement according to the present invention.

40 [0010] The solution of the present invention advantageously provides a multi-band frequency synthesiser for communication on UMTS/GSM/GPRS frequency bands of compact design, fast switching behaviour, with no spurious spectra produced in an unwanted frequency band, and which shows low phase noise. Furthermore, by dispensing complex components in the design, a cost-effective solution is achieved.

45 [0011] Additional advantageous features of the present invention are claimed in the respective sub-claims.

50 [0012] The frequency synthesiser sub-units advantageously comprise a frequency divider for transforming the signal of the reference frequency source into a scaled-down signal which frequency value represents the reference frequency divided by an integer value, and the frequency synthesiser sub-units comprise further advantageously a phase locked loop frequency synthesiser for transforming the scaled-down signal into a signal which frequency is an integer multiple of the scaled-down signal.

55 [0013] A frequency mixer preferably mixes a signal from the second synthesiser sub-unit with a signal derived from the auxiliary signal for forming a signal in a range of the third type of frequency band or for forming a precursor for deriving a signal in a range of the fourth type of frequency band. Advantageously, a frequency divider divides the frequency of the auxiliary signal by an integer value before it is being applied to the frequency mixer.

[0014] In a preferred embodiment of the present invention, a frequency divider derives a signal in a range of the

fourth type of frequency band from a signal supplied by the frequency mixer by dividing the frequency of the signal supplied by the frequency mixer with an integer value.

[0015] A low pass filter is preferably used to eliminate harmonics created in the circuitry for generating signals used for a signal with a frequency in a range of the third or the fourth type of frequency band, and further preferably a low pass filter is used to eliminate harmonics created by the frequency divider providing the signals for the fourth type of frequency band.

[0016] The frequencies of the first type of frequency band may advantageously take on values from one of the frequency intervals ranging from 1900 MHz to 1980 MHz and 2010 MHz to 2025 MHz, the frequencies of the second type of frequency band may further advantageously take on values from the frequency interval ranging from 2110 MHz to 2170 MHz, the frequencies of the third type of frequency bands may preferably take on values from one of the frequency bands situated within an interval ranging from 1710 MHz to 1990 MHz, and further preferably, the frequencies of the fourth type of frequency bands may take on values from one of the frequency bands situated within an interval ranging from 880 MHz to 960 MHz.

[0017] The present invention may advantageously be implemented on mobile phones particularly for wireless cellular telecommunication networks,

[0018] In the following description, the present invention is explained in more detail with respect to special embodiments and in relation to the enclosed drawings, in which

20 Figure 1 shows the schematic circuit diagram of a frequency synthesiser sub-unit according to the present invention,

Figure 2 shows the schematic circuit diagram of a multi-band frequency synthesiser according to the present invention,

25 Figure 3 is a frequency plan of the multi-band frequency synthesiser shown in Fig. 2, and

Figure 4 shows the reference sensitivity level versus frequency defining the limitations for outband emissions for all frequency bands to be considered.

30 [0019] Figure 1 illustrates the principles of a frequency synthesiser sub-unit 10 used in the multi-band frequency synthesiser according to the present invention. The signals generated at an output 18 of a sub-unit constitute either directly a frequency of a respective frequency band or constitute an auxiliary frequency for further processing.

[0020] The inputs 17 of all sub-units are supplied with a reference frequency signal f_r from a reference crystal oscillator. In a first stage, the reference frequency f_r is scaled down to $I_D = f_r / R$ by an integer division coefficient R set at 35 the programmable frequency divider 12 by digital control code. The following phase locked loop frequency synthesiser 11 then adjusts the output frequency of a voltage controlled oscillator (VCO) 15 to the desired value.

[0021] The phase locked loop frequency synthesiser 11 works in principle like a frequency multiplier with a frequency raster f_D . This is achieved by using a programmable integer frequency divider 16 in the feedback line of the phase locked loop frequency synthesiser which scales down the output frequency of the VCO 15 by the division coefficient N .

40 [0022] The phase locked loop frequency synthesiser comprises a phase frequency detector 13 which provides an output voltage $u_o(t)$ proportional to the phase angle deviation between the input frequency I_D and the down-scaled output frequency f_o/N . This output voltage $u_o(t)$ is filtered by a low pass filter 14 before being supplied to the VCO 15. The filter characteristics of low pass 15 are wide enough to allow a fast switching of the output frequency or quick lock time, respectively, when changing the between frequency bands and narrow enough to block off higher frequencies 45 which otherwise would cause phase noise in the output spectrum of the voltage controlled oscillator. The output frequency f_o of the VCO 15 is a function of the value of the filtered output voltage $u_o(t)$ which is supplied to it. In the feedback loop of the phase locked loop frequency synthesiser 11, this output frequency signal f_o is scaled down with an appropriate integer value N to a value equal that of f_D for being applied to the phase frequency detector 13. There 50 it is compared with the original frequency signal f_D to produce the control voltage $u_o(t)$ for the VCO 15. After termination of the transient processes, the value of the output frequency f_o is thus controlled by the code division coefficient N set at the programmable frequency divider 16 of the feedback loop according to the equation:

$$f_o = N \times f_D = \frac{N}{R} \times f_r;$$

55 with N and R as integers.

According to equation 1, the output frequency f_o is an integer multiple of the input frequency f_D or, in other words, f_D defines a frequency raster for f_o . A change in the output frequency is achieved by changing the division coefficient N ,

a process sufficiently fast to allow fast frequency hopping. Neither spurious spectra nor additional phase noise that are so characteristic for fractional-N frequency synthesisers are produced by this procedure so that no extra filters for a post-processing of the output spectra of the phase locked loop frequency synthesiser 11 are required.

5 [0023] A multi-band frequency synthesiser unit 200 according to the present invention is shown in Figure 2. It comprises the three phase lock loop frequency synthesisers PLL1 211, PLL2 221, and PLL3 231 of the type described with reference to Figure 1. Two of them, namely PLL1 and PLL2 work for UMTS up- and down-links, while the third (PLL3) produces in combination with PLL2 and additional mixers and frequency dividers all necessary frequencies for triple band GSM/GPRS functionalities. Each phase lock loop frequency synthesiser is preceded by a programmable frequency divider which receives its input frequency signal from a reference frequency source 201 like e.g. a crystal oscillator providing a stabilised oscillation frequency of 19.2 MHz.

10 [0024] Different from the first phase lock loop frequency synthesiser 211, the second phase lock loop frequency synthesiser 221 operates alternately at two different input frequencies supplied from the preceding phase frequency divider 222. The UMTS down-link frequencies are provided with the first input frequency, the intermediate frequency signals forming a basis for the provision of the GSM/GPRS bands are provided with second input frequency. This positively affects the settling time and phase noise for the GSM/GPRS frequency bands.

15 [0025] The third phase lock loop frequency synthesiser 231 is narrow banded (about 24 MHz) and processes a high frequency at the phase frequency detector 233 which reduces the settling time and the phase noise. The divider 237 at its output scales down the output frequency and also the frequency steps of the phase lock loop frequency synthesiser 231 by a factor of M_1 . This reduces the phase noise even further.

20 [0026] The multi-band frequency synthesiser shown in Figure 2 has four output terminals 219, 229, 239, and 249, each providing signal for a certain frequency band. The assignment of the frequency bands to the respective output terminals is shown in table 1.

25	Terminal	Frequency Band	Frequency Range / MHz
30	219	TDD1, FDD-T _x	1900 - 1980
	219	TDD2	2010 - 2025
35	229	FDD-R _x	2110 - 2170
	239	DCS-T _x	1710 - 1785
	239	DCS-R _x	1805 - 1880
40	239	PCS-T _x	1850 - 1910
	239	PCS-R _x	1930 - 1990
	249	GSM-T _x	880 - 915
	249	GSM-R _x	925 - 960

Table 1: Frequency range assignments for output terminals of the multi-band frequency synthesiser 200

45 [0027] The synthesiser branch 202 of the multi-band frequency synthesiser 200 providing the first output terminal 219 produces signals with frequencies in the UMTS frequency bands 'FDD transmitter' (FDD-T_x) and TDD1 (1900 - 1980 MHz), and TDD2 (2010-2025 MHz), respectively. The programmable frequency divider 212 scales down the reference frequency f_r by a factor R_1 , whereby the integer R_1 is set to the value of 96 as a result of which a frequency signal f_{D1} of 0.2 MHz is produced at its output. The code division coefficient R_1 is set, like for all other programmable frequency dividers used in the circuit representation of Figure 2, by means of a control code CC.

50 [0028] The function of a phase lock loop frequency synthesiser has already been described with reference to figure 1. The integer code division coefficient N_1 applied to the feedback line of PLL1 succeeding the programmable frequency divider 212 is programmably adjustable for producing the desired frequency of the output signal f_{o1} according to equation 1. For the TDD1/FDD-T_x frequency bands, the values of N_1 range from 9500 to 9,900, whereby incrementing N_1 by a value of 1 results in an incrementation of f_{o1} by a value of 0.2 MHz. For the TDD2 frequency band, the values of N_1 have to be adjusted in the interval beginning with 10,050 and ending at 10,125.

55 [0029] When operating in the UMTS frequency band 'FDD receiver' (PDD-R_x) ranging from 2110 to 2170 MHz, the

output signal f_{o2} of PLL2 221 is supplied to the second output terminal 229. To this end, the programmable frequency divider 222 of the second synthesiser branch 203 of the multi-band frequency synthesiser 200 scales down the reference frequency f_r by a factor R_2 being with a value of 96 equal to R_1 . The resulting signal is then multiplied in PLL2, whereby the multiplication factor is controlled by the code division coefficient N_2 applied to the feedback loop. The values of N_2 range from 10,550 to 10,850. The frequency raster of the output frequency f_{o2} or the possible incremental changes of f_{o2} , respectively, are hereby fixed to steps of 0.2 MHz.

5 [0030] The second synthesiser branch 203 of the multi-band frequency synthesiser 200 can be operated in a second mode to produce frequencies appropriate for deriving the GSM/GPRS frequency bands. In this second mode, the programmable frequency divider 222 scales down the reference frequency f_r by a factor $R_2 = 6$, thereby supplying PLL2 with an input frequency signal of $f_{D2} = 3.2$ MHz. This frequency is multiplied by PLL2 to frequencies in the range of 2110 to 2390 MHz with a frequency raster of 3.2 MHz. The large frequency steps guarantee a short settling time together with a low phase noise also for the GSM/GPRS frequency signals. The second synthesiser branch 203 of the multi-band frequency synthesiser works in both modes according to the principles described with reference to Figure 1.

10 [0031] To derive the GPRS frequency bands from the signal provided at the output of PLL2, the signal is mixed in frequency mixer 227 with an auxiliary frequency $f_{o3}/8$ provided from the third synthesiser branch 204 of the multi-band frequency synthesiser 200. The frequency mixer 227 acts in combination with the low pass filter 238 as a subtractor according to the equation:

$$20 f_{GPRS} = f_{o2} - \frac{f_{o3}}{8};$$

whereby f_{o3} represents the frequency of the output signal from PLL3 231.

25 [0032] For providing the auxiliary frequency signal f_{o3} in the third synthesiser branch 204 of the multi-band frequency synthesiser 200, the reference frequency f_r is scaled down by R_3 , having a value of 12. The resulting signal with a frequency of 1.6 MHz is then supplied to PLL3 231, where it is transformed to a signal f_{o3} with a frequency around 3200 MHz by setting the division coefficient N_3 of the programmable frequency divider 236 to a constant value of 2000. Before being applied to an input of the frequency mixer 227, f_{o3} is scaled down to 400 MHz in the digital frequency divider 237 by a factor M_1 of fixed value 8. The GPRS frequency bands are thus provided by adjusting f_{o2} to an appropriate value. A detailed relation between the division coefficient N_2 , the frequency band of the output signal f_{o2} of PLL2 and the desired GPRS frequency band is given in table 2.

N ₂	f _{o2}	frequency band	frequency range
657 - 683	2110 - 2185	DCS-T _x	1710 - 1785
689 - 713	2205 - 2280	DCS-R _x	1805 - 1880
703 - 722	2250 - 2310	PCS-T _x	1850 - 1910
728 - 747	2330 - 2390	PCS-R _x	1930 - 1990

45 Table 2: Relations between parameters of PLL3 and respective GSM bands; frequencies are given in MHz

[0033] The low pass filter 238 blocks off harmonics originating from the mixing process in the frequency mixer 227 and also harmonics having their source in one of the voltage controlled oscillators 225 (VCO2) or 235 (VCO3). The 50 signal provided at the output of low pass filter 238 to the third output 239 of the multi-band frequency synthesiser 200 is thus given by equation 2 above.

[0034] The frequencies for the GSM bands provided at the fourth output terminal 249 of the multi-band frequency synthesiser 200 are derived from the output of low pass filter 238 acting as a precursor by further scaling down the precursor frequency by a factor M_2 of fixed value 2, and subsequent filtering in low pass filter 242 to eliminate harmonics produced in the digital frequency divider 241. The frequencies at the output of the low pass filter 238 must be divisible by 2 for a simple construction of the digital frequency divider 242.

[0035] A detailed relation between the division coefficient N_2 , the frequency band of the output signal f_{o2} of PLL2 and the desired GSM frequency band is given in table 3.

N_1	f_{ω}	precursor range	frequency band	frequency range
675 - 697	2160 - 2230	1760 - 1830	GSM-T _x	880 - 915
703 - 725	2250 - 2320	1850 - 1920	GSM-R _x	925 - 960

Table 3: Relations between parameters of PLL2, precursor frequency range, and respective GPRS bands; frequencies are given in MHz

[0036] There is no need to post-process the output signals $f_{\omega 1}$ and $f_{\omega 2}$ of PLL1 and PLL2, respectively, by low pass filters like for the GSM/GPRS frequency bands, because the coding used for UMTS like e.g. CDMA (Code Division Multiple Access) spreads the information contained in a particular signal of interest over a much greater bandwidth than the original signal, thereby enhancing the interference immunity of the signal transmission. Spurious signals from harmonics of VCO1 or VCO2 will therefore not degrade quality of a signal transmission.

[0037] It has to be noted, that the UMTS-up-link frequencies are produced independent of the GSM/GPRS up- and down-link frequencies to guarantee a GSM monitoring during an UMTS call in uncompressed mode.

[0038] In a preferred embodiment an ADF4213 Integer-N Dual RF/IF PLL Frequency Synthesizer 1.0 GHz/3 GHz or a different but compatible phase locked loop (PLL) frequency synthesiser from Analog Devices (AD) or from a further supplier are used as phase lock loop frequency synthesisers 211, 221, and 231. Devices with one or up to four PLL synthesiser in one package can be used. PLL synthesisers from Analog Devices are preferred due to their very short settling times achieved with the built-in so-called Fastlock Mode, but devices from other manufacturers may be used as well.

[0039] In a further preferred embodiment of the present invention, all digital circuit elements are implemented in one ASIC (Application Specific Integrated Circuit), while only for the voltage controlled oscillators 215, 225, and 235, the mixer 227, the filters 238 and 242, and the reference frequency source 201 discreet or integrated circuit devices are used.

[0040] A frequency plan of a multi-band frequency synthesiser 200 according to the present invention is given in Figure 3. Except for UMTS frequency bands which show a high interference immunity, none of the frequencies produced in one of the VCO's which also includes the harmonics, must not fall into a reception or a transmission band of the multi-band frequency synthesiser 200 to fulfil the requirements of GSM standard 0505. This is achieved by using frequencies for the VCO's which lay fairly above the GSM/GPRS frequencies. Further, also the harmonics of VCO3 235 when down-scaled by digital frequency divider 237 must not fall into a GSM/GPRS reception or transmission band.

[0041] Further, none of the frequencies of a VCO's equals that of another VCO to prevent a direct lock which would result in a serious decrease of the spectrum performance. VCO's with a small tuning range show a better spectrum performance than those with a wide tuning range, and are therefore preferably used in a multi-band frequency synthesiser according to the present invention. This is particularly true for VCO3 235. VCO's with a maximum frequency equal or not far above the used maximum frequency are preferred, for the power consumption of a VCO increases with its maximum frequency specification which in turn will reduce the recharging intervals of a mobile terminal.

[0042] For keeping low pass filters 238 and 242 small, image frequencies requiring complex filtering have to be avoided. The maximum values of $f_{\omega 3}/M_1$ must therefore not exceed 0.1 $f_{\omega 2}$ to achieve an effective saturation of spurious components at the frequency mixer 227 output.

[0043] The frequency plan of figure 3 further shows the filter characteristic of loop filter 214 (LPF1) indicating that its bandwidth is sufficiently broad to allow a fast switching of frequencies at VCO 215, but is also sufficiently narrow to prevent phase noise in the output spectra of the phase locked loop frequency synthesiser 211.

[0044] The frequencies of the VCO's are chosen in such a manner, that neither the frequencies themselves nor a harmonic produced in the process falls within a band with maximum requirements for spurious suppression. For the third synthesiser branch 204 of the multi-band frequency synthesiser 200 according to the present invention the said has to be applied to the frequencies and harmonics of signals produced by VCO3 235 divided by M_1 . In this manner, the requirements for outband emissions according to GSM standard 0505 as shown in Figure 4 are fulfilled with minimal design effort by low circuit complexity.

Claims

1. A frequency synthesiser arrangement for generating signals with frequencies for UMTS and GSM/GPRS frequency bands, comprising

- 5 - a reference frequency source (201) for providing a signal of constant reference frequency,
- a first frequency synthesiser sub-unit (202) for transforming the signal of the reference frequency source (201) into a signal with a frequency in a range of a first type of frequency band,
- a second frequency synthesiser sub-unit (203) for transforming the signal of the reference frequency source (201) into a signal with a frequency in a range of a second type of frequency band,

10 **characterised in,**

15 that said second frequency synthesiser sub-unit (203) further transforms the signal of the reference frequency source (201) into a signal with an intermediate frequency, and a third frequency synthesiser sub-unit (204) transforms the signal of the reference frequency source (201) into an auxiliary signal with a fixed frequency which is used together with the signal of intermediate frequency for generating signals with frequencies in a range of a third and of a fourth type of frequency band.

20 2. A frequency synthesiser arrangement according to claim 1,

characterised in,

25 that a frequency synthesiser sub-unit (202, 203, 204) comprises a frequency divider (212, 222, 232) for transforming the signal of the reference frequency source (201) into a scaled-down signal which frequency value represents the reference frequency divided by an integer value.

30 3. A frequency synthesiser arrangement according to claim 2,

characterised in,

35 that a frequency synthesiser sub-unit (202, 203, 204) comprises a phase locked loop frequency synthesiser (211, 221, 231) for transforming said scaled-down signal into a signal which frequency is an integer multiple of the scaled-down signal.

40 4. A frequency synthesiser arrangement according to claim 1, 2 or 3,

characterised in,

45 that a frequency mixer (227) mixes a signal from the second synthesiser sub-unit (203) with a signal derived from the auxiliary signal for forming a signal in a range of the third type of frequency band or for forming a precursor for deriving a signal in a range of the fourth type of frequency band.

5. A frequency synthesiser arrangement according to claim 4,

characterised in,

50 that a frequency divider (237) divides the frequency of the auxiliary signal by an integer value before it is being applied to the frequency mixer (227).

6. A frequency synthesiser arrangement according to one of the claims 1 to 5,

characterised in,

45 that a frequency divider (241) derives a signal in a range of the fourth type of frequency band from a signal supplied by the frequency mixer (227) by dividing the frequency of said signal supplied by the frequency mixer (227) with an integer value.

7. A frequency synthesiser arrangement according to one of the claims 4 to 6,

characterised in,

50 that a low pass filter (238) is used to eliminate harmonics created in the circuitry for generating signals used for a signal with a frequency in a range of the third or the fourth type of frequency band.

8. A frequency synthesiser arrangement according to one of the claims 6 to 7,

characterised in,

55 that a low pass filter (242) is used to eliminate harmonics created by the frequency divider (241) providing the signals for the fourth type of frequency band.

9. A frequency synthesiser arrangement according to one of the claims 1 to 8,

characterised in,
that the frequencies of said first type of frequency band take on values from one of the frequency intervals ranging from 1900 MHz to 1980 MHz and 2010 MHz to 2025 MHz,
the frequencies of said second type of frequency band take on values from the frequency interval ranging from 5 2110 MHz to 2170 MHz,
the frequencies of said third type of frequency bands take on values from one of the frequency bands situated within an interval ranging from 1710 MHz to 1990 MHz, and
the frequencies of said fourth type of frequency bands take on values from one of the frequency bands situated within an interval ranging from 880 MHz to 960 MHz.

10 10. A mobile terminal for use with UMTS and GSM/GPRS frequency bands comprising a frequency synthesiser arrangement according to one of the claims 1 to 9.

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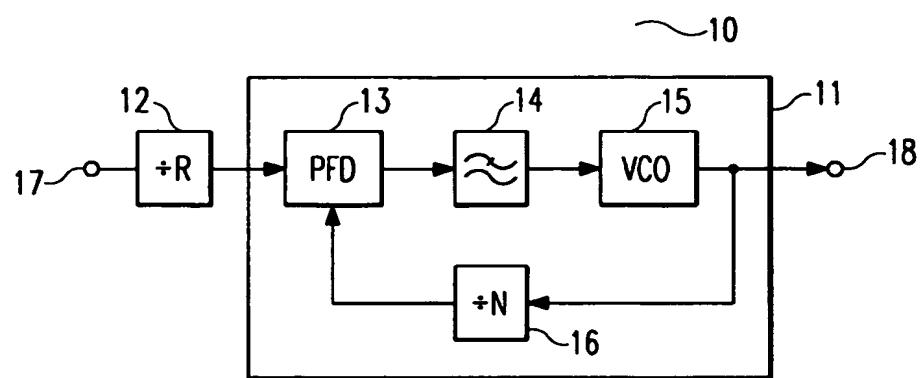


Fig. 1

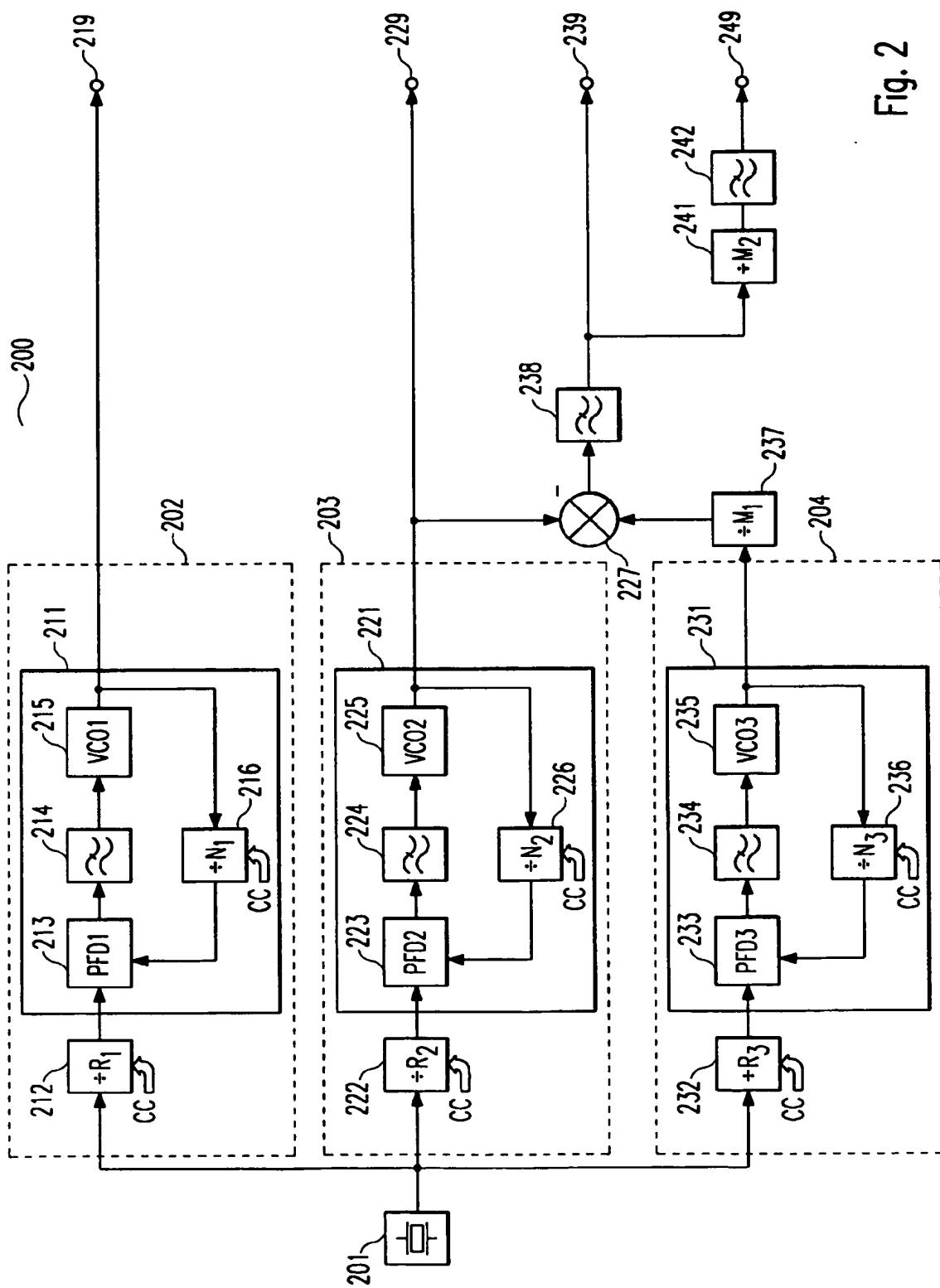


Fig. 2

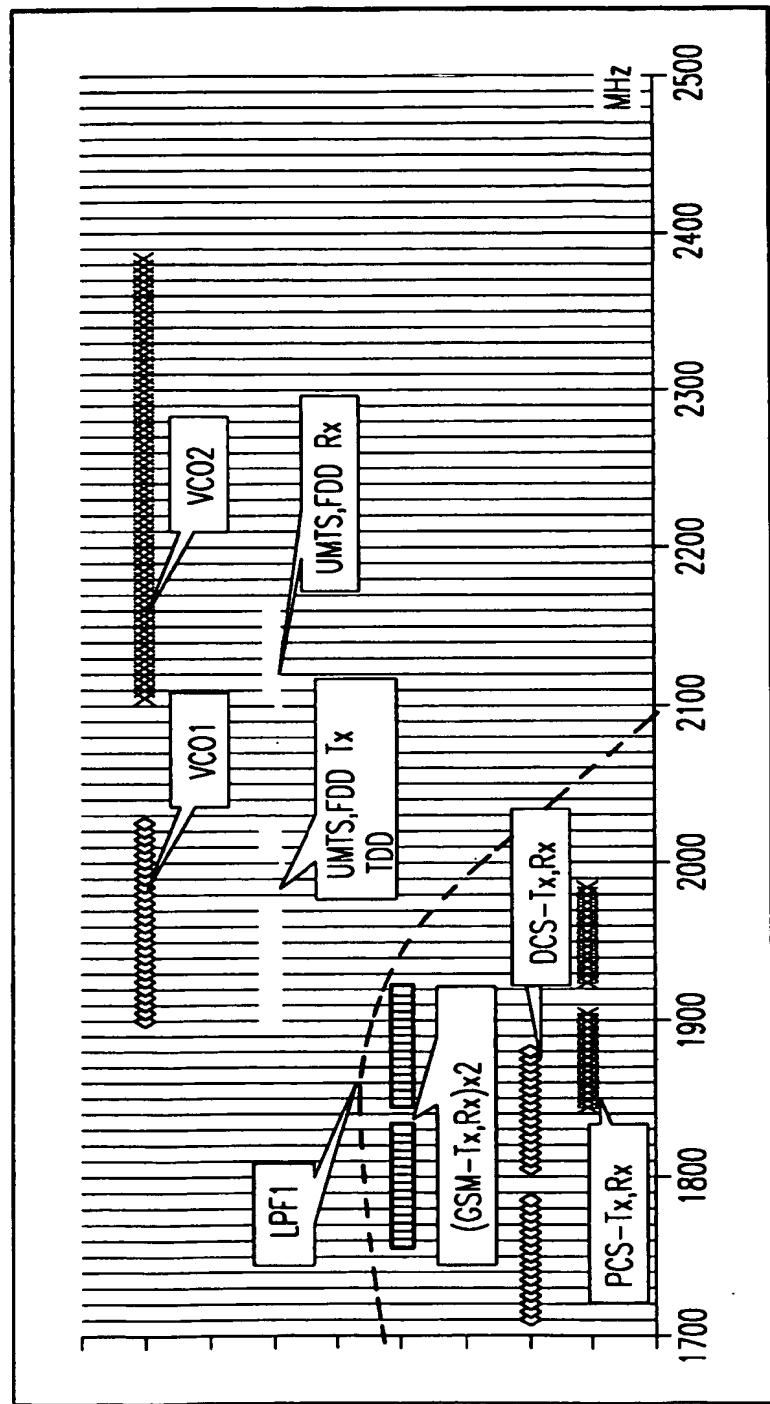


Fig. 3

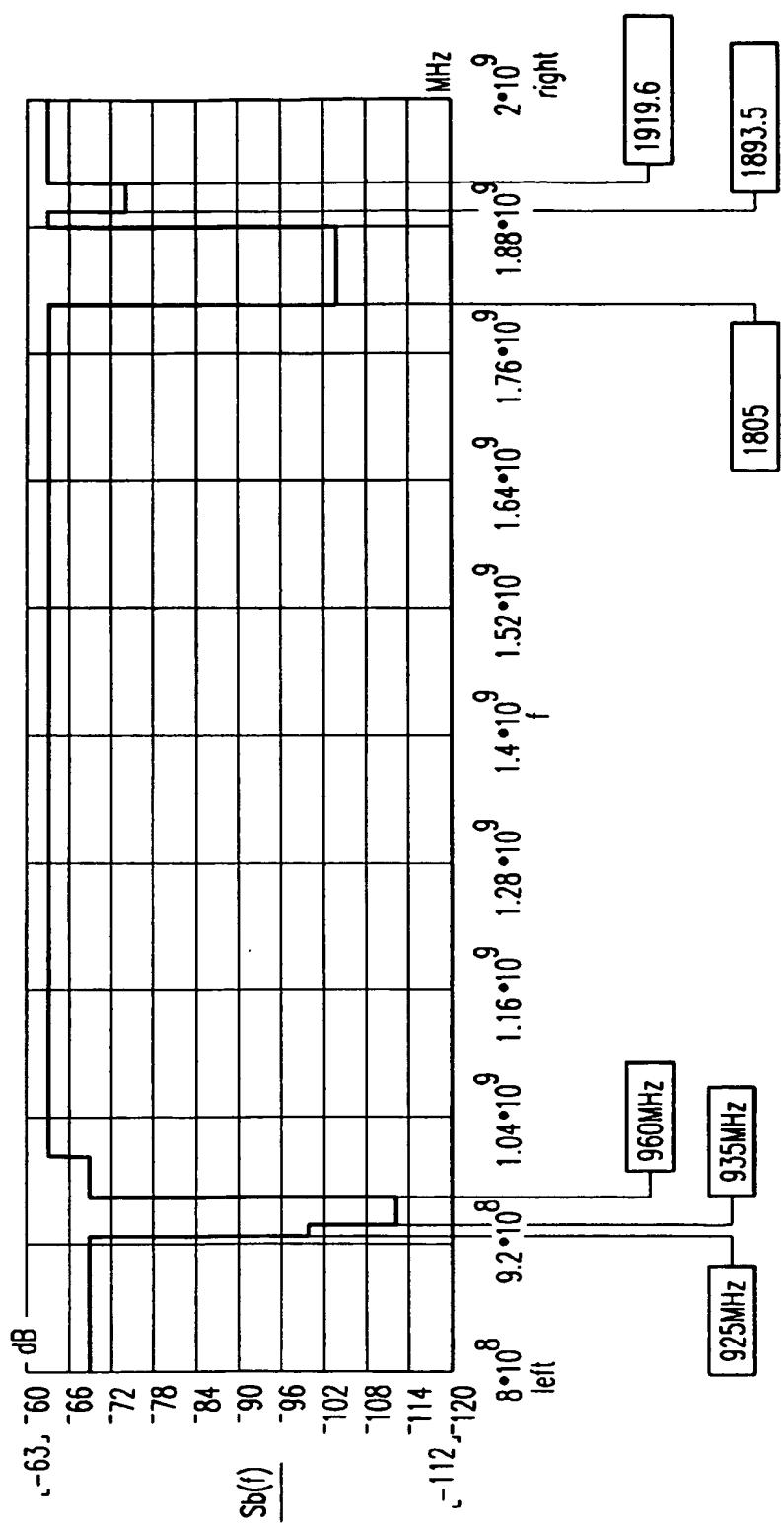


Fig. 4



DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 5 408 201 A (URIYA SUSUMU) 18 April 1995 (1995-04-18) * column 7, line 66 - column 10, line 49; figures 5,6 *	1-4,7,10	H03B21/00 H04B1/40
X	EP 1 148 654 A (INFINEON TECHNOLOGIES AG) 24 October 2001 (2001-10-24) * page 4, line 5 - page 6, line 36; figures 1,2 *	1-5,10	
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The present search report has been drawn up for all claims			
Place of search	Date of completion of the search	Examiner	
THE HAGUE	30 October 2002	Balbinot, H	
CATEGORY OF CITED DOCUMENTS		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	
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ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 01 12 9616

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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